IN THE CLAIMS

1. (Currently amended) A memory device, comprising:

a plurality of memory cells to store data;

a data output buffer adapted to operate in a first mode and a second mode, wherein the first mode operates to output ~~for outputting~~ data stored in the memory cells;

a comparator to determine failure of the memory cells to store the data, by comparing the stored data with expected data; and

a fail bit counter for counting the number of those of the memory cells that fail to store data, and for outputting a fail code representing the counted number of the fail bits to the data output buffer, wherein the second mode of the data output buffer operates to output the fail code.

2. (Original) The device of claim 1, further comprising:

a fail bit detecting circuit for detecting those of the memory cells that fail to store data, and for updating the fail bit counter accordingly.

3. (Original) The device of claim 2, in which

the fail bit detecting circuit includes a latch for storing signals that encode the counted number of failed bits.

4. (Original) The device of claim 2, in which

the fail bit detecting circuit is in a data output path between the memory cells and the data output buffer.

5. (Cancelled)

6. (Currently amended) The device of claim 2, further comprising:

an expected data input buffer circuit for receiving externally supplied expected data bits, ~~and~~

in which the ~~fail bit detecting circuit~~ comparator is adapted to compare the externally supplied expected data bits with test bits stored in the memory cells to detect those of the memory cells that fail to store data.

7. (Previously presented) The device of claim 6, in which

during a test operation, data bits identical to the externally supplied expected data bits have been stored in the memory cells.

8. (Currently amended) A nonvolatile semiconductor memory device, comprising:

an array of memory cells arranged in the form of a matrix having rows and columns;

a row decoder circuit for selecting one of the rows in accordance with a row address;

a column select circuit for selecting some of the columns in response to a column address and outputting data bits corresponding the selected columns;

an expected data input buffer circuit for receiving expected data bits supplied from the outside via input/output pins in response to a fail bit detecting command signal;

a fail bit detecting circuit for operating in response to the fail bit detecting command signal, receiving the expected data bits and the selected data bits, determining failure of the memory cells to store the data, by comparing the selected data bits with the expected data bits, and determining whether the data bits selected by the column select circuit include fail bits, and outputting fail flag signals according to the determination result;~~-and~~

a fail bit counter and latch circuit for counting the number of the fail bits of the data bits stored in the selected row memory cells in response to the fail flag signals from the fail bit detecting circuit and outputting a fail code representing the counted number of the fail bits; and

a data output buffer adapted to operate in a first mode and a second mode, wherein the first mode operates to output data stored in the memory cells and the second mode operates to output the fail code.

9. (Cancelled)

10. (Previously presented) The device of claim 8, in which

the fail bit detecting circuit receives data bits sent via the column select circuit in synchronization with read-out enable signals.

11. (Original) The device of claim 8, in which

the fail bit counter and latch circuit is initialized when the fail bit detecting command signal is transitioned from a low level to a high level.

12. (Original) The device of claim 8, further comprising:

a data output buffer circuit connected to the input/output pins, and

in which the data output buffer circuit prevents the data bits selected by the column select circuit from being sent to the input/output pins during an activation period of the fail bit detecting command signal.

13. (Previously presented) The device of claim 12, in which

the data output buffer circuit allows a fail code from the fail bit counter and latch circuit to be sent to the input/output pins in synchronization with clock signals during the activation period of the fail bit read-out command signal.

14. (Original) The device according to claim 8, further comprising:

a data output buffer circuit connected to the input/output pins, and

in which the data output buffer circuit allows the data bits selected by the column select circuit to be sent to the fail bit detecting circuit and prevents the data bits selected by the column select circuit from being sent to the input/output pins during an activation period of the fail bit detecting command signal.

15. (Original) The device of claim 14, in which

the data input/output buffer circuit allows a fail code from the fail bit counter and latch circuit to be sent to the input/output pins in synchronization with the clock signal during the activation period of the fail bit read-out command signal.

16. (Original) The device of claim 8, in which

the fail bit detecting circuit generates first and second fail flag signals.

17. (Original) The device of claim 16, in which the fail bit detecting circuit

activates the first fail flag signal when one of the inputted data bits is a fail bit, and

activates the first and second fail flag signals simultaneously when at least 2 bits of the inputted data bits are fail bits.

18. (Original) The device of claim 16, in which

each of the first and second fail flag signals is activated as a clock signal during the activation period of the read-out enable signal.

19. (Original) The device of claim 16, in which the fail bit counter and latch circuit includes:

a counter for outputting first and second count signal in response to the first fail flag signal, in which the first count signal is activated in pulse corresponding to the first activation of the first fail flag signal and the second count signal is activated in pulse corresponding to the second activation of the second fail flag signal;

a combination circuit for outputting a set signal by combination of the second count signal and the second fail flag signal; and

a register for activating first fail status signal when the first count signal is activated and second fail status signal when the set signal from the combination circuit is activated.

20. (Original) The device of claim 19, in which the fail bit counter and latch circuit further includes:

a pulse generator for generating a pulse signal, when the fail bit detecting command signal is activated and the counter and the register are initialized by the pulse signal.

21. (Currently amended) A method for detecting fail bits in a nonvolatile semiconductor memory device, comprising:

storing test data in memory cells of the device;

inputting expected data in an expected data buffer of the device;

comparing the stored expected data with the stored test data to determine failure of the memory cells to store data; ~~and~~

creating a fail code to register~~ing~~ failure occasions in which the inputted expected data does not correspond with the stored test data;

outputting data stored in the memory cells from a data output buffer; and

outputting the fail code from the data output buffer.

22. (Original) The method of claim 21, in which

the test data is identical to the expected data.

23. (Original) The method of claim 21, further comprising:
receiving a fail bit detecting command signal to initiate the comparing.

24. (Original) The method of claim 21, further comprising:
counting the registered failure occasions in a counter of the device.

25. (Original) The method of claim 24, further comprising:
outputting to an output data buffer of the device signals encoding a number of the counted failure occasions.

26. (Original) The method of claim 24, further comprising:
initializing the counter.

27. (Currently amended) A method for detecting fail bits in a nonvolatile semiconductor memory device having an array of memory cells, comprising:
detecting data stored in the array in response to a read command signal;
selecting some of the detected data bits in response to a column address;
determining whether the selected data bits each matches corresponding expected data bits applied from the outside;
counting the number of data bits unmatched in the determining step;
storing a fail code determined according to the counted number;
incrementing the column address; ~~and~~
performing repeatedly the selecting, determining, counting and storing steps until a maximum of the column address is reached;
outputting data stored in the memory cells from a data output buffer; and
outputting the fail code from the data output buffer.

28. (Original) The method of claim 27, further comprising:
receiving a fail bit detecting command signal to initiate the determining.

29. (Original) The method of claim 27, further comprising:
outputting the stored fail code in response to a fail bit read-out command signal, until a maximum of the column address is reached.

30. (Original) The method of claim 27, further comprising:

initializing a fail bit counter and latch circuit in response to the fail bit detecting signal when the fail bit detecting signal is activated after the detecting step has been completed, and the fail code is stored in the fail bit counter and latch circuit.

31. (Previously presented) A nonvolatile semiconductor memory device, comprising:

an array of memory cells arranged in the form of a matrix having rows and columns;

a row decoder circuit for selecting one of the rows in accordance with a row address;

a column select circuit for selecting some of the columns in response to a column address and outputting data bits corresponding the selected columns;

an expected data input buffer circuit for receiving expected data bits supplied from the outside via input/output pins in response to a fail bit detecting command signal;

a fail bit detecting circuit for operating in response to the fail bit detecting command signal, receiving the expected data bits and the selected data bits, determining failure of the memory cells to store the data, by comparing the selected data bits with the expected data bits, and determining whether the data bits selected by the column select circuit include fail bits, and outputting fail flag signals according to the determination result, the fail bit detecting circuit generating first and second fail flag signals; and

a fail bit counter and latch circuit for counting the number of the fail bits of the data bits stored in the selected row memory cells in response to the fail flag signals from the fail bit detecting circuit and outputting a fail code representing the counted number of the fail bits, the fail bit counter and latch circuit including:

a counter for outputting first and second count signal in response to the first fail flag signal, in which the first count signal is activated in pulse corresponding to the first activation of the first fail flag signal and the second count signal is activated in pulse corresponding to the second activation of the second fail flag signal;

a combination circuit for outputting a set signal by combination of the second count signal and the second fail flag signal; and

a register for activating first fail status signal when the first count signal is activated and second fail status signal when the set signal from the combination circuit is activated.

32. (Previously presented) The device of claim 31, in which the fail bit counter and latch circuit further includes:

a pulse generator for generating a pulse signal, when the fail bit detecting command signal is activated and the counter and the register are initialized by the pulse signal.

33. (New) The device of claim 1, wherein the data stored in the memory cells is blocked from being output while operating in the second mode.

34. (New) The device of claim 1, wherein the data output buffer includes a first circuit path for data stored in the memory cells and a second circuit path for the fail code, wherein only the first or the second circuit path is operational, responsive to a test command.